Examiner has previously considered the dimensional relationship of the first and second semiconductor chip and the circuit board. The specified dimensional relationship was implicit in unamended claim 10 and claims 11 and 12. The dimensional relationship is also clearly shown in Fig. 1, 4, and 8, which have been previously considered by the Examiner. If this application is not allowed, Applicant requests that the amendment be entered as it would significantly reduce the issues for appeal.

Claim Rejections Under 35 U.S.C. § 112

Claim 12 is rejected under 35 USC § 112, first paragraph, as non-enabling. This rejection is traversed, and reconsideration and withdrawal thereof respectfully requested.

Although Applicants believe that claim 12 was fully enabled, this rejection is moot as claim 12 has been canceled.

Claim Rejections Under 35 U.S.C. § 103

Claim 10 is rejected under 35 USC § 103(a) as being unpatentable over alleged admitted prior art (APA) in view of Fukui et al. (U.S. Patent No. 6,100,594) and Williams et al. (U.S. Patent No. 5,665,996).

Claims 11 and 12 are rejected under 35 USC § 103(a) as being unpatentable over Fukui et al. in view of Williams et al. and further in view of Bertin et al. (U.S. Patent No. 6,294,406).

These rejections are traversed, and reconsideration and withdrawal respectfully requested. The following is a comparison between the instant invention as claimed, and the cited prior art.

Claim 10 requires a first semiconductor chip positioned on the circuit board, wherein the semiconductor chip is sized and configured to be smaller than the circuit board, so that the chip is confined within an outer periphery of the circuit board. A second semiconductor chip is positioned on the first semiconductor chip, wherein the second semiconductor chip is sized and

configured to be smaller than the first semiconductor chip so that the second semiconductor chip is confined within an outer periphery of the first semiconductor chip. The circuit board has a first pad, a second pad spaced away from the first pad in a direction along the outer periphery of the semiconductor chip, and a wire connecting between the first pad and the second pad on a surface of the circuit board supporting the first semiconductor chip. The wire is printed on the circuit board together with the first pad and the second pad. The second semiconductor chip has a third pad positioned adjacent to the second pad but away from the first pad on the circuit board. The second pad on the circuit board and the third pad on the second semiconductor chip are electrically connected through a bonding wire so that the third pad on the second semiconductor chip is electrically connected with the first pad on the circuit board through the wire, the second pad on the circuit board, and the wire on the circuit board.

The Examiner asserts that the APA discloses a semiconductor device including a circuit board 102, semiconductor chips 110, 112, connection pads 104-1, 104-2, etc., spaced away from each other, and bonding wires 116. The Examiner acknowledges that the APA fails to specify the second pad spaced away from the first pad in a direction along the outer peripheral edge of the chip and a wire being printed on the board, the wire connecting the first and second pad. The Examiner asserts that FIG. 7(a) and 9(a) of Fukui teach forming first and second pads spaced away from each other in any direction along or perpendicular to the outer peripheral edges of the chip. The Examiner further relies on Williams to provide the bonding wire connecting desired wiring portions. The Examiner concludes that it would have been obvious to incorporate a circuit board having first and second pads such that the second pad is spaced away from the first pad in a direction along the outer peripheral edge of the chip and a wire printed on the board connecting the first and second pads to reduce the wire bonding defects and bonding wire length wire-shorting problems.

The APA, Fukui, and Williams, whether taken alone, or in combination, fail to suggest the claimed semiconductor device. None of the references suggests the circuit board with a first pad and a second pad spaced away from the first pad in a direction along an outer periphery of the first semiconductor chip, and a wire connecting between the first pad and the second pad, as required by claim 10. Fukui, in FIG. 7(a) teaches two pads spaced away from each in a **direction extending away from** the outer peripheral edge of the semiconductor chip, not along the outer periphery of the chip, as required by claim 10.

The combination of the APA, Fukui, and Williams further fails to suggest the semiconductor device wherein a first semiconductor chip is sized and configured so that it is confined within the outer periphery of the circuit board, and the second semiconductor chip is sized and configured so that it is confined within an outer periphery of the first semiconductor chip, and where the circuit board has spaced apart pads along the outer periphery of the first semiconductor chip connected by a wire, as required by claim 10. The combination of the cited references also fails to suggest the claimed device with a third pad on the second semiconductor chip positioned adjacent to the second pad but away from the first pad on the circuit board, and the second pad on the circuit board and third pad on the second semiconductor chip electrically connected through a bonding wire, so that the third pad is electrically connected to the first pad, as required by claim 10.

Typically, when a semiconductor device has a first chip provided on a circuit board and a second chip provided on the first chip, the connecting line between the top smaller chip and the base circuit board tend to extend obliquely, which may cause unwanted crossing and extension of the bonding wires. However, the claimed arrangement of the pads on the circuit board solves such problems.

It would further not be obvious to combine the Williams' teaching of a bonding wire into the devices taught by the APA and Fukui. Williams discloses stitch bonding that repeatedly bonds to the surface of a die in a snake-like pattern (column 2, lines 37 *at seq.*). Williams teaches using stitch bonding to short out the resistance of a metal layer. Williams does not teach using wire bonding to connect a second pad on a circuit board to a third pad on a second semiconductor chip, as required by claim 10.

The mere fact that references can be combined or modified does not render the resulting combination obvious unless the prior art also suggest the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990). There is no suggestion in Williams to connect a second pad on circuit board and a third pad on a second semiconductor chip via a bonding wire. Further there is no suggestion in Fukui to form on the circuit board a first pad and a second pad spaced away from the first pad in a direction along an outer periphery of first semiconductor chip, as required by claim 10.

Furthermore, Williams also teaches that stitch bonding suffers from numerous problems. As explained by Williams, stitch bonding requires specialized bonding equipment, repeated bonding steps of close spacing subjects the die to high mechanical stress, and multiple bonds also takes longer than normal bonding resulting in reduced throughput.

A prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention. *W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), *cert. denied,* 469 U.S. 851 (1984). As a whole, Williams clearly teaches away from using stitch bonding. Williams' teaching is potent evidence of non-obviousness. One of ordinary skill in the art would not be motivated to connect a second pad and a third pad using a bonding wire in view of the teaching of Williams.

Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge readily available to one of ordinary skill in the art. *In re Kotzab*, 217 F.3d 1365, 1370 55 USPQ2d 1313, 1317 (Fed. Cir. 2000); *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992); *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988). There is no suggestion in the cited references to form a first pad and a second pad spaced away from the first pad in a direction along an outer periphery of a first semiconductor chip on a circuit board, and to form a wire connecting the first pad and the second pad on the circuit board.

The requisite motivation to support the ultimate legal conclusion of obviousness under 35 U.S.C. § 103 is not an abstract concept, but must stem from the applied prior art as a whole and realistically impel one having ordinary skill in the art to modify a specific reference in a specific manner to arrive at a specifically claimed invention. *In re Deuel*, 51 F.3d 1552, 34 USPQ2d 1210 (Fed. Cir. 1995); *In re Newell*, 891 F.2d 899, 13 USPQ2d 1248 (Fed. Cir. 1989). Accordingly, the Examiner is charged with the initial burden of identifying a source in the applied prior art for the requisite realistic motivation. *Smiths Industries Medical System v. Vital Signs, Inc.*, 183 F.3d 1347, 51 USPQ2d 1415 (Fed. Cir. 1999); *In re Mayne*, 104 F.3d 1339, 41 USPQ2d 1449 (Fed. Cir. 1997). There is no motivation in the cited references to a form a first pad and a second pad spaced away from the first pad in a direction along an outer periphery of first semiconductor chip on a circuit board and connected by a wire, wherein the first semiconductor chip is confined within an outer periphery of the circuit board and a second semiconductor chip is formed on the first semiconductor chip and confined within an outer periphery of the first semiconductor chip.

The only teaching of the claimed semiconductor device is found in Applicants' disclosure. However, the teaching or suggestion to make a claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicants' disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). The Examiner's conclusion of obviousness is not supported by any factual evidence. The Examiner's retrospective assessment of the claimed invention and use of unsupported conclusory statements are not legally sufficient to generate a case of *prima facie* obviousness. The motivation for modifying the prior art must come from the prior art and must be based on facts.

As regards the Bertin reference, Bertin does not cure the deficiencies of the APA, Fukui and Williams references. The APA, Fukui, Williams, and Bertin, whether taken alone or in combination, fail to suggest the claimed semiconductor device. The cited references do not suggest a semiconductor device comprising a circuit board having a first pad and a second connected to the first pad, but spaced away from the first pad in a direction along an outer periphery of the first semiconductor chip, and a second pad on the circuit board connected to a third pad on a second semiconductor chip, as required by claim 10, wherein the second semiconductor chip is formed on the first semiconductor chip.

The rejection of claims 11 and 12 is moot as these claims have been canceled.

In light of the amendments and remarks above, this amendment should be entered, the application allowed, and the case should be passed to issue. If there are any questions regarding this Amendment or the application in general, a telephone call to the undersigned would be appreciated to expedite the prosecution of the application.

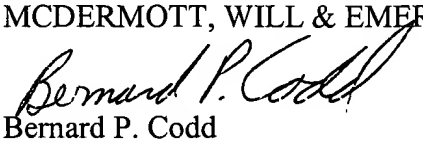
To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including

extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Attached hereto is a marked-up version of the changes made to the specification by the current amendment. The attached page is captioned "VERSION WITH MARKINGS TO SHOW CHANGES MADE."

Respectfully submitted,

MCDERMOTT, WILL & EMERY



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Claim 10 has been amended as follows:

10. (Amended) A semiconductor device, comprising:

a circuit board; [and]

a first semiconductor chip positioned on the circuit board, the first semiconductor chip being sized and configured to be smaller than the circuit board so that the first semiconductor chip on the circuit board is confined within an outer periphery of the circuit board; and

a second semiconductor chip positioned on the first semiconductor chip, the second semiconductor chip being sized and configured to be smaller than the first semiconductor chip so that the second semiconductor chip on the first semiconductor chip is confined within an outer periphery of the first semiconductor chip; wherein

(a) the circuit board has a first pad, a second pad spaced away from the first pad in a direction along [an outer peripheral edge] the outer periphery of the first semiconductor chip, and a wire connecting between the first pad and the second pad on a surface of the circuit board supporting the first semiconductor chip, the wire being printed on the circuit board together with the first pad and the second pad;

(b) the second semiconductor chip has a third pad positioned adjacent to the second pad but away from the first pad on the circuit board; and

(c) the second pad on the circuit board and the third pad on the second semiconductor chip are electrically connected through a bonding wire, so that the third pad on the second semiconductor chip is electrically connected with the first pad on the circuit board through the

bonding wire, the second pad on the circuit board, and the wire on the circuit board.

Claims 11 and 12 have been canceled.